UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,990	08/26/2003	Jin-Acon Lee	8021-170 (SS-19644-US)	2486

22150 7590 02/07/2007

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
CONNOLLY, MARK A	
ART UNIT	PAPER NUMBER
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/647,990	LEE ET AL.	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,13,22,27,30,32,33 and 36-41* is/are allowed.

6)☒ Claim(s) *1-7,9-12,14-21,23-26,28,29,31,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 have been presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9-12, 14-21, 23-26, 28-29, 31 and 34-35 rejected under 35 U.S.C. 103(a) as being unpatentable over Dai[1] in view of Wong-Insley[2] in view of Tobias[3].

4. Referring to claim 1, Dai teaches the invention substantially including:

a. selecting a power-off standby mode [col. 1 lines 35-45].

b. transmitting a working context with respect to at least one hardware module mounted on a chip to a predetermined memory, and storing the working context in the predetermined memory [col. 4 lines 30-35].

c. transmitting the working context stored in the predetermined memory to a memory outside the chip, and storing the working context in the outside memory [fig. 3 and col. 4 lines 22-35].

d. executing the power-off standby mode [col. 4 lines 30-35].

Although Dai suggests the external memory as being a self suspend RAM or second cache, it is not explicitly taught that the external memory is non-volatile. Dai does openly admit

---

[1] As cited in the previous office action.
[2] As cited in the previous office action.
[3] As cited in the previous office action.

the importance on reducing power consumption. With that in mind, Dai only teaches two power consumption modes: high power dissipation state and low power dissipation state. Even when Dai is in a low power dissipation state, it is still necessary to supply power to the context memory when removing power from the core in order to preserve the context even if the system remains idle or unused for an extended period of time. Wong-Insley teaches a means to conserve additional power by storing context in a non-volatile memory [col. 11 lines 10-47]. In particular, Wong-Insley teaches a sleep state wherein the context must be stored in a "self-refresh" or "battery-backed RAM" or in other words, a power mode wherein power is still required to maintain context information. This power mode is interpreted as being similar to the low power dissipation state in Dai since the processors in both systems do not operate and power is required to preserve context. Wong-Insley further teaches a suspend state which consumes even less power than the low power dissipation state and sleep state above. By storing context information into non-volatile memory, power to the CPU and memory can be removed completely. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Wong-Insley into the Dai system because it would provide a means for Dai to conserve additional power. It is obvious that Dai could be modified by either backing the context from the SSRAM or second cache into non-volatile memory or by replacing the SSRAM or second cache with a non-volatile memory.

Although the Dai – Wong-Insley system does not explicitly teach a system-on-a-chip (SOC) Wong-Insley does teach that power management is an important issue with existing computing devices. The examiner took official notice that SOC design is an extremely well known concept in the art that integrates a plurality of system components into a single chip,

which was acknowledged by applicant[4]. It would have been obvious to one of ordinary skill in the art at the time of the invention to realize the teachings of Dai and Wong-Insley in an SOC design because it would reduce the size and cost of the Dai – Wing-Insley system while providing power management to SOC devices.

As it is known, SOC devices integrate a plurality of hardware devices including a microprocessor into a single chip. Tobias teaches a plurality of devices integrated into a single chip similar to an SOC wherein the plurality of devices on the chip must store their context before entering a suspend mode [col. 1 lines 14-40; col. 5 lines 58-60 and col. 7 lines 3-9]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Dai – Wong-Insley system to further store the context of SOC peripheral devices because Tobias teaches the need to preserve all context data before entering a suspend state and powering down. By preserving all context data into the memories taught in the Dai – Wong-Insley system, it would provide the system with the ability to completely remove power from the SOC since all context data would be safely preserved thus providing an optimal amount of power savings in addition to allowing the SOC to return to a higher power state without having to reset the context of the embedded peripherals in the SOC.

5. Referring to claim 2, Wong-Insley teaches that when the system wakes up it returns to its previous execution state [col. 13 lines 25-32].

6. Referring to claim 3, NAND and NOR flash memories are well known in the art and it would have been obvious by design choice to use either as the non-volatile memory.

---

[4] See REMARKS filed 1/16/07.

7. Referring to claim 4, although the Dai–Wong-Insley–Tobias system teaches the predetermined memory as being internal, the location of the memory is not critical to the success of the system. In fact, Wong-Insley suggests that context can be stored into a DRAM [col. 11 lines 27-30]. Due to the size of DRAM, it would have been obvious to locate it off chip in order to maintain a small footprint for the SOC.

8. Referring to claim 5, Dai teaches that the power to the processor core is disconnected [col. 4 lines 22-35].

9. Referring to claim 6, Dai teaches returning the processor core to its operating state [270 fig. 2C and col. 5 lines 41-54].

10. Referring to claim 7, this is rejected on the same basis as set forth hereinabove. In addition, Dai teaches an on-die logic circuit integrated into the processor that controls power to the microprocessor [col. 4 lines 5-9]. It is interpreted that since the preservation of the context data is directly dependent upon the power state of the core, that the on-die logic circuit, which is part of the microprocessor, would also have control over saving the context data in the predetermined and non-volatile memories as well.

11. Referring to claim 9, again, Dai teaches an on-die logic circuit integrated into the processor that controls power to the microprocessor [col. 4 lines 5-9]. Since the on-die logic circuit controls the storing of context data to memory, it is obvious that the on-die logic circuit would output the predetermined command signal for initiating the storing.

12. Referring to claims 10-12 these are rejected on the same basis as set forth hereinabove.

13. Referring to claims 14-21, 23-24 these are rejected on the same basis as set forth hereinabove.

14. Referring to claim 25, the on-die logic circuit in Dai which controls power and operation as stated above is interpreted as the at least one hardware module.

15. Referring to claims 26, 28-29 and 31, these are rejected on the same basis as set forth hereinabove. Dai, Wong-Insley and Tobias teach the method and therefore teach the system performing the method.

16. Referring to claim 34, Wong-Insley teaches removing power from the non-volatile memory [col. 11 lines 35-43].

17. Referring to claim 35, this is rejected on the same basis as set forth hereinabove.

Allowable Subject Matter

18. Claims 8, 13, 22, 27, 30, 32-33 and 36-41 are allowed.

Response to Arguments

19. Applicant's arguments filed 1/16/07 have been fully considered but they are not persuasive.

20. In the remarks, applicants argue in substance that 1) Dai fails to teach saving hardware working context for more than one hardware module, 2) Wong-Insley teaches saving hardware states which are different than the context data claimed, 3) the microcontroller in Tobias differs from a microprocessor and 4) Tobias and Dai fail to address variable sized working context suitable for a microprocessor which may use variable stack sizes and indorect pointers to various chip-level resources.

21. In response to arguments 1-3 that argue against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re*

Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In particular, the Dai–Wong-Insley–Tobias system teaches a chip which has embedded on it a microprocessor and peripheral devices which can store their context into a first memory while in a first low power mode and transfer the context data to another memory when in a second low power mode. In addition, Tobias teaches that the microcontroller comprises a microprocessor [col. 1 lines 29-33].

22. In response to argument 4 which argues that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., using variable stacks and indirect pointers) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Connolly
Examiner
Art Unit 2115

mc
February 1, 2007